Lorenzo Di Tucci

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WORK EXPERIENCE

03/2017 – 07/2017
Visiting Researcher
Lawrence Berkeley National Laboratory (LBNL) – Berkeley, CA - USA

Worked as a visiting researcher at Berkeley Lab on a hardware implementation of the merAligner sequence aligner on FPGA, using Chisel HDL and Xilinx/Altera FPGAs, under the supervision of Steven Hofmeyr and David Donofrio.

10/2016–Present
Teaching Assistant
Politecnico di Milano – Milan, Italy

TA for Fundamentals of Computer Science course at Politecnico di Milano (Prof. Cristiana Bolchini)

09/2016–04/2017
Research Assistant
NECST Lab – Politecnico di Milano, Milan - Italy

I worked as a research assistant for Politecnico di Milano at NECST Lab, under the supervision of Marco D. Santambrogio. My main focuses regarded High Performance Computing, reconfigurable architectures and Biological Applications.

06/2015–12/2015
FPGA Engineer Intern
Xilinx Research Labs – Dublin, Ireland

Worked as an FPGA engineer under the supervision of Dr. Michaela Blott. My main tasks involved the design, acceleration and benchmark of High Performance Computing applications targeting hardware accelerators such as FPGAs, GPUs, and co-processors.

01/2015–05/2015
Research Assistant
Electronic Visualization Laboratory (EVL) , University of Illinois at Chicago – Chicago IL

Worked with Monika Marko in the CHECK (Coordination for Healthcare for Complex Kids) project, and with Prof. Angus G. Forbes in the project “Imaging Macondo – A Pocket full of Memories”.

08/2013–present
Soccer Referee
Centro Sportivo Italiano (CSI) – Milano Italy

Official soccer matches direction, technical meeting and working with sport courts in opening game records.

08/2013–09/2013
Web developer
Libit Srl, Zola Predosa (BO) - Italy

Web designer and developer for the website of the company.

04/2012
Web Developer
Centro Sportivo Italiano (CSI) – Milano Italy

Web designer and developer of a website that allows referees to acquire, develop and manage data about members of the association, create reports and general-purpose committee for various internal uses.

EDUCATION AND TRAINING

05/2017–Present — Ph.D. in Information Technology — EQF level 8

Politecnico di Milano, Milano (Italy)

The main objectives of my current research are the exploration of new hardware/software codesign methodologies for FPGA-based High Performance Computing infrastructures, and the development of HUG (Hardware for hUman Genomics). It is a web platform for the research in the field of personalized medicine. HUG aims at providing the user with performant and power efficient applications executed on hardware accelerators (GPU/FPGA) and efficient data visualization algorithms to interpret the results.

10/2013–07/2016 — Master degree in Computer Science Engineering(103/110) — EQF level 7

Politecnico di Milano, Milano (Italy)

The thesis "FPGA-based High Performance Architecture for Computational Biology: the case of the Smith-Waterman algorithm" involved the design and benchmark of a hardware architecture based on Systolic Array to perform the Smith-Waterman Algorithm.

01/2014–08/2016 — Master of Science in Computer Science (average GPA: 3.7/4.0) — EQF level 7

University of Illinois at Chicago (UIC), Chicago (United States)

The thesis "Efficient High Performance FPGA-based Applications Design via SDAccel" proposed the design of two applications from the biomedical fields using the new Xilinx SDAccel framework.

09/2010–07/2013 — Bachelor Degree in Computer Science Engineering (99/110) — EQF level 6

Politecnico di Milano, Milano (Italy)

The thesis project (horse fever), consisted in the implementation of a client-server game using Java.

PERSONAL SKILLS

Mother tongue(s) Italian

Other language(s)

	UNDERSTANDING		SPEAKING		WRITING
	Listening	Reading	Spoken interaction	Spoken production	
English	C1	C1	C1	C1	C1
	TOEFL IBT (106/120)				

Digital competence

Good knowledge of Windows, Linux and Mac OS

Knowledge of C, Chisel HDL, Java and OpenCL

Basic Knowledge of C++, Verilog and Python

Good knowledge of the Xilinx Vivado Suite, SDAccel and Git.

Other languages: HTML, PHP, JS(d3.js), MySQL

Awards

Winner of the Hipeac Collaboration Grant 2017 for the collaboration with LBNL

Winner of the Xilinx Open Hardware Contest 2016 in Student FPGA Category (http://www.openhw.eu/2016-finalists.html)

MAIN PROJECTS

2017 — Design of a Systolic Array for the Smith-Waterman Algorithm using Chisel HDL

LBNL, Berkeley CA

This work is an extension of the work I have published at DATE 2017. It involved the design of a hardware architecture for performing the two steps of the Smith-Waterman algorithm. For the first step, it has been defined a Systolic Array of processing elements, and the FSMs to control AXI4 transactions to and from DDR3. For the second step, it has been used the HMC to perform random reads/write to memory.

2017 CAOS: CAD as an Adaptive Open-platform Service

Politecnico di Milano, Italy

A framework that aims at facilitating the development of algorithms for FPGA platforms in the field of HPC, while being open to external contributions. Within this project, I developed in Python an algorithm to optimize the usage of local memory for the functions to be accelerated on FPGA.

2016 ProFAX

Politecnico di Milano, Italy

This project involved the acceleration of a protein folding algorithm on FPGA. It has been developed at NECST Lab and it is the winning entry of the Xilinx Open Hardware 2016.

2015 Imaging Macondo – A Pocket full of memories

EVL – University of Illinois at Chicago IL

This project has been developed at UIC, in collaboration with George Legrady, Paul Murray and Angus Forbes. This project has been shown at the international book fair of Bogota (Colombia). It is composed of a web-app, and a visualization app running a SOP (Self organizing maps) algorithm to cluster pictures, and visualize them. The aim of this project was to represent Macondo, the city described in - One hundred years of solitude book by the nobel prize Gabriel Garcia Marquez.

Relevant Projects:

UIC: Computer Graphics final project: http://lorenzoditucci.com/cs488Project/

UIC: Visualization and Visual Analytics Project: Visualization of data regarding the city of Chicago using JS and d3.js at different level of abstraction.

From C to Hardware: Performance and Power considerations: optimize the ratio of performance over power consumption of linear algebra application starting from a high level representation in C.

ADDITIONAL INFORMATION

Publications

Lorenzo Di Tucci, Davide Conficconi, Alessandro Comodi, Steven Hofmeyr, David Donofrio and Marco D Santambrogio. A parallel, energy efficient hardware architecture for the meraligner on FPGA using chisel hcl. In Parallel and Distributed Processing Symposium Workshops (IPDPSW), 2018 IEEE International, pages tbd. IEEE, 2018.

Emanuele Del Sozzo, **Lorenzo Di Tucci**, and Marco D Santambrogio. A highly scalable and efficient parallel design of n-body simulation on fpga. In Parallel and Distributed Processing Symposium Workshops (IPDPSW), 2017 IEEE International, pages 241–246. IEEE, 2017.

Lorenzo Di Tucci, Giulia Guidi, Sara Notargiacomo, Luca Cerina, Alberto Scolari, and Marco D Santambrogio. Hugenomics: A support to personalized medicine research. In Research and Technologies for Society and Industry (RTSI),2017IEEE 3rd International Forum on, pages 1–5. IEEE, 2017.

Lorenzo Di Tucci, Kenneth O'Brien, Michaela Blott, and Marco D Santambrogio. Architectural optimizations for high performance and energy efficient smith-waterman implementation on fpgas using opencl. In 2017 Design, Automation & Test in Europe Conference & Exhibition (DATE), pages 716–721. IEEE, 2017

Lorenzo Di Tucci, Marco Rabozzi, Luca Stornaiuolo, and Marco D Santambrogio. The role of cad frameworks in heterogeneous fpga-based cloud systems. In 35th IEEE International Conference on Computer Design (ICCD 2017), page tbp. IEEE, 2017.

Kenneth O'Brien, **Lorenzo Di Tucci**, Gianluca Durelli, and Michaela Blott. Towards exascale computing with heterogeneous architectures. In 2017 Design, Automation & Test in Europe Conference & Exhibition (DATE), pages 398–403. IEEE, 2017.

Giulia Guidi, **Lorenzo Di Tucci**, and Marco D Santambrogio. Profax: A hardware acceleration of a protein folding algorithm. In Research and Technologies for Society and Industry Leveraging a better tomorrow (RTSI), 2016 IEEE 2nd International Forum on, pages 1–6. IEEE, 2016.

Giulia Guidi, Enrico Reggiani, **Lorenzo Di Tucci**, Gianluca Durelli, Michaela Blott, and Marco D Santambrogio. On how to improve fpga-based systems design productivity via sdaccel. In Parallel and Distributed Processing Symposium Workshops, 2016 IEEE International, pages 247–252. IEEE, 2016